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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,074	11/19/2003	Peter Dean Swartz	GENSP052	1073

22434 7590 11/24/2006

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EXAMINER
RICHER, AARON M

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 11/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,074	SWARTZ ET AL.	
	Examiner	Art Unit	
	Aaron M. Richer	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-15,18-25 and 29-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-15,18-25 and 29-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed September 12, 2006 have been fully considered but they are not persuasive.

2. As to claim 1, applicant argues that progressive scan data in Perlman is not converted into data that is appropriate for an interlaced display. However, it is recognized in the art that a progressive image displayed on an interlaced display is *inherently* interlaced. An interlaced display is only capable of displaying half of a progressive image at one time. See for instance http://reviews.cnet.com/4520-6029_7-6160720-1.html, which describes how a CRT at high resolutions scans odd-numbered lines and then even-numbered lines. Therefore the output of an interlaced display, such as that rendered in fig. 3b, is an interlaced image, since it displays one field at a time instead of one frame. The flicker filter cited by examiner previously is part of the "interlace unit" that converts the progressive scan data to better be displayed on an interlaced display. If the display were truly displaying progressive data, this flicker filter would be unnecessary, as there would be no sequential fields creating flicker.

3. Applicant further argues that Perlman does not use a frame rate conversion to synchronize synchronize source material to a frame rate consistent with a display, as is required by claim 1. Examiner notes that one skilled in the art would recognize a deinterlacer, as in fig. 3a, to change a frame rate of video. Perlman states in p. 2, section 0024 that deinterlacing is done using deinterlacing techniques known in the art. One skilled in the art would recognize this deinterlacer to be interpreted as some sort of

line doubler (see http://en.wikipedia.org/wiki/Line_doubler). By doubling each line, or using another technique which interpolates between lines, each interlaced field becomes a progressive frame. Since, in interlaced format, a frame is equal to two fields, by deinterlacing, the frame rate is doubled, as now each field has become one frame.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 8, 11-15, 19, 22-25, 30, 33, and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Perlman (U.S. Publication 2002/0135696).

6. As to claims 1, 12, and 23, Perlman discloses a video processor for providing a single synchronized video stream having a single display video format to a first display device having a first set of display attributes from a number of input video streams of different video formats, comprising:

a number of ports each of which is configured to receive one of the input video streams at a corresponding input video stream clock rate (fig. 2; p. 2, section 0020; multiple communication modules for receiving data are disclosed; these read on ports);

a number of configurable image converter units each coupled to an associated one of the ports for converting the corresponding input video stream to a corresponding converted video stream having the single display video format that is based upon the

set of display attributes (fig. 3a; fig. 3b; the units are configurable based on input format and attributes of a display);

and a frame rate conversion unit configured to synchronize each converted data stream to a selected output frame rate (fig. 3a, the deinterlacer changes the frame rate of the interlaced video to be compatible with a progressive display).

7. As to claims 2, 13, and 34, Perlman discloses a configurable real time video processor wherein when a second display unit having a second set of display attributes replaces the first display unit, then the system controller uses the second set of display attributes received from the second display unit to reconfigure the configurable image converter units and the configurable frame rate conversion unit accordingly (fig. 3a-3b; conversion is reconfigured if an interlaced display is replaced with a progressive one or vice versa).

8. As to claims 3, 14, and 25, Perlman discloses a processor comprising:

an image compositor unit arranged to combine the converted data streams to form a composited data stream (fig. 3a, element 312);

an image enhancer unit arranged to enhance the composited data stream to form an enhanced data stream (p. 2-3; section 0026; an anti-aliased composited stream reads on an "enhanced" data stream);

a display unit interface arranged process the enhanced data stream to form the display data (fig. 3a, element 314);

and a memory unit bi-directionally coupled to each of the image converter units and the image compositor arranged to store selected portions of selected ones of the

data streams from the image converter units and to provide the selected portions to the image compositor as needed (fig. 2, element 216; p. 2-3; section 0026; buffers hold the foreground and background pixels to be combined).

9. As to claims 4, 15, and 24, Perlman discloses a processor wherein the output frame is locked to any of the input video data stream clock rates (fig. 3a, 3b; the frame is locked to either the interlaced or non-interlaced clock rate for compatibility with the display).

10. As to claims 8, 19, and 30, Perlman discloses

a video receiver port arranged to receive video data at a video clock rate (fig. 2, element 230);

a bi-directional network interface arranged to receive network data from network applications on a network, and transmit data to the network from the real time video processor at a network data clock rate (fig. 2, element 220; a clock rate for data transfer is inherent);

a user interface port arranged to receive user input commands at a user interface clock rate (p. 2, sections 0022-0025; a user interface is disclosed; also note "interactive" content in fig. 2).

11. As to claims 11, 22, and 33, Perlman discloses

an interlacer unit arranged to interlace a progressive scan image when the display unit is an interlaced type display unit (p. 3, section 0028; the flicker filter formats a progressive image for an interlaced display);

and a progressive scan bypass unit arranged to bypass the interlacer when the display unit is a progressive scan type display unit (fig. 3a, no interlacer is used).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 7, 18, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perlman in view of Naegle (U.S. Publication 2004/0012577).

15. As to claims 7, 18, and 29, Perlman does not expressly discloses a processor wherein the display frame rate is a free running frame rate. Naegle, however, does disclose a video processor with a free running frame rate. The motivation for this is to provide a larger set of pixel clock frequencies for various formats (p. 1, paragraph

0014). It would have been obvious to one skilled in the art to modify Perlman to use a free running frame rate in order to support more diverse formats as taught by Naegle.

16. Claims 9, 20, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perlman.

17. As to claims 9, 20, and 31, Perlman does not disclose a processor as an integrated circuit. Official notice has been taken of the fact that graphics processors on integrated circuits are well-known in the art (see MPEP 2144.03). It would have been obvious to one skilled in the art to modify Perlman to use an integrated circuit in order to make the graphics processor smaller and reduce production costs.

18. Claims 10, 21, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perlman in view of Leyvi (U.S. Publication 2003/006752).

19. As to claims 10, 21, and 32, Perlman does not expressly disclose basing conversion on a set of Extended Display Identification Data (EDID) attributes. Leyvi, however, discloses a conversion process in which EDID is used to read attributes of a display (p. 3, paragraph 0025). The motivation for this is to easily determine whether a format is compatible with a display (p. 3, paragraph 0025). It would have been obvious to one skilled in the art to modify Perlman to read attributes of a display in EDID format in order to determine format compatibility as taught by Leyvi.

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron M. Richer whose telephone number is (571) 272-7790. The examiner can normally be reached on weekdays from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AMR
11/17/06

KEE M. TUNG
SUPERVISORY PATENT EXAMINER